



Deinterlace Algorithm for Arm9/Arm11/Arm12 Release Notes

RELEASE ENGINEER:	Zhenyong Chen
PROJECT(S):	Deinterlace
CUSTOMER(S):	L-PDK, W-PDK
DATE:	June 26, 2008

ABSTRACT:

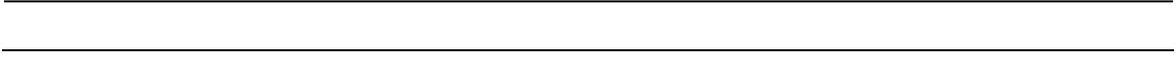
KEYWORDS:

APPROVED:

WANG ZENING

AUTHOR	SIGN-OFF SIGNATURE #1	SIGN-OFF SIGNATURE #2
Zhenyong Chen		
SIGN-OFF SIGNATURE #3	SIGN-OFF SIGNATURE #4	SIGN-OFF SIGNATURE #5

ERROR! UNKNOWN DOCUMENT PROPERTY NAME.



ERROR! UNKNOWN DOCUMENT PROPERTY NAME.

COPYRIGHT © 2008, FREESCALE, INC.
ALL RIGHTS RESERVED. PRESENCE OF COPYRIGHT NOTICE IS NOT AN ACKNOWLEDGEMENT OF PUBLICATION.

Revision History

VERSION	DATE	AUTHOR	CHANGE DESCRIPTION
1.0	2007-12-24	Zhenyong Chen	Creation of Release Note for REL1.0
1.1	2008-03-04	Zhenyong Chen	New deinterlace method (frame group) added
1.2	2008-05-04	Zhenyong Chen	Arm9 content added
1.3	2008-06-26	Zhenyong Chen	Modify API for version string

Table of Contents

1	Read Me First	1
1.1	Requirements.....	1
1.1.1	System Requirements.....	1
1.1.2	Target Requirements	2
1.1.3	Equipment Requirements	2
1.2	Upgrading From the Previous Release.....	2
1.3	Problem Reporting Instructions	3
2	Release Content	4
3	What's New	5
3.1	New Features.....	5
3.2	New Regressions	5
3.3	Fixed Features	5
4	Release Description	6
4.1	Supported Features	6
4.2	Feature Regressions.....	6
4.3	Limitations	6
5	Summary of Changes	7
5.1	New Works.....	7
5.2	Fixed Defects.....	7
5.3	Workarounds	7
6	Known Issues	8
Appendix A	Release History	9

1 Read Me First

The purpose of this document is to provide deinterlace algorithm release information, mainly focus on:

- Package contents
- Feature
- Changes
- Known issues

1.1 Requirements

1.1.1 System Requirements

i.MX27 requirements:

MCIMX27	
ARM Core	ARM926EJ-S
Frequency(MHz)	399 MHz
L1 Cache Size	I=16 KB, D=16 KB
L1 Cache Setting	Writeback
L2 Cache Size	N/A
L2 Cache Setting	N/A
External Memory Interface Width	32 bits
External Bus Width	32 bits
External Bus Frequency	133 MHz
Core:Bus Ratio	3:1
Ext. Memory Type	DDR

i.MX31 requirements:

MCIMX31	
ARM Core	ARM1136J-S
Frequency(MHz)	533 MHz
L1 Cache Size	I=16 KB, D=16 KB
L1 Cache Setting	Writeback
L2 Cache Size	128 KB

L2 Cache Setting	Writeback
External Memory Interface Width	32 bits
External Bus Width	32 bits
External Bus Frequency	133 MHz
Ext. Memory Type	DDR

Elvis requirements:

ELVIS	
ARM Core	Coretex-A8
Frequency(MHz)	400 MHz
L1 Cache Size	I=16 KB, D=16 KB
L1 Cache Setting	Writeback, Write Allocation
L2 Cache Size	256 KB
L2 Cache Setting	Writeback, Write Allocation
External Memory Interface Width	32 bits
External Bus Width	32 bits
External Bus Frequency	166 MHz
Ext. Memory Type	DDR

Software requirements:

- N/A

1.1.2 Target Requirements

Target requirement:

- i.MX27, i.MX31 or Elvis

1.1.3 Equipment Requirements

N/A

1.2 Upgrading From the Previous Release

Two deinterlace method added: frame group SAD plus Bob; frame group SAD plus 4-tap filter.

1.3 Problem Reporting Instructions

Please submit CRs on the ClearQuest system:

<http://cq.freescale.net/cqweb/login>

Database :

ENGR : Production DB

Parent Bins :

MAD Bins & Project

MAD Components: Multimedia

MAD-MMCODEC

2 Release Content

Release package can be retrieved at:

<http://compass.freescale.net/go/180740750>

DELIVERABLE	LOCATION	STATUS
Documentation	Root/docs/deinterlace	Updated
Application Interface header file	Root/ghdr/	Updated
RVDS libraries and test applications	Root/release/	Updated
Source code and Makefiles for library including optimized assembler for RVDS libraries. *	Root/src/deinterlace Root/src/deinterlace/c_src Root/src/deinterlace/asm_arm Root/src/deinterlace/asm_arm_gnu Root/src/deinterlace/hdr	Updated
Source code and Makefiles for test application for RVDS libraries.	Root/test/deinterlace/applications/PerformanceTest Root/test/deinterlace/middleware/cpp_src Root/test/deinterlace/middleware/hdr	Updated

Note *: Only authorized audiences can access this content.

3 What's New

3.1 New Features

Version 1.2 offers these new features:

- Support detailed version information

3.2 New Regressions

None

3.3 Fixed Features

None

4 Release Description

4.1 Supported Features

Version 1.2 offers these features:

- Support optimization for Arm1136
- Support optimization for Cortex
- Support Arm9
- Support chroma format 4:2:0, 4:2:2, 4:4:4
- Support multiple deinterlacing algorithms

4.2 Feature Regressions

N/A.

4.3 Limitations

- Input top field and bottom field should be interleaved;
- Chroma format should be one of 4:2:0, 4:2:2, and 4:4:4;
- Picture width should be 16x.

5 Summary of Changes

This section lists in details the list of CRs changed from the previous release.

IDENTIFIER	HEADLINE	STATE
ENGR81880	[DEINTERLACE] Modify API for detailed version description	Resolved

5.1 New Works

IDENTIFIER	HEADLINE	STATE

5.2 Fixed Defects

IDENTIFIER	HEADLINE	STATE

5.3 Workarounds

N/A.

6 Known Issues

IDENTIFIER	HEADLINE	STATE

Appendix A Release History

Provide the ordered list (**latest release first**) of all releases since the beginning.

RELEASE VERSION	DATE	DESCRIPTION
1.3	2008-06-26	Modify API for version information
1.2	2008-05-04	Add Arm9 content for REL1.1
1.1	2008-03-04	Update Release Note for REL1.1
1.0	2007-12-24	Creation of Release Note for REL1.0
